Fig. 1

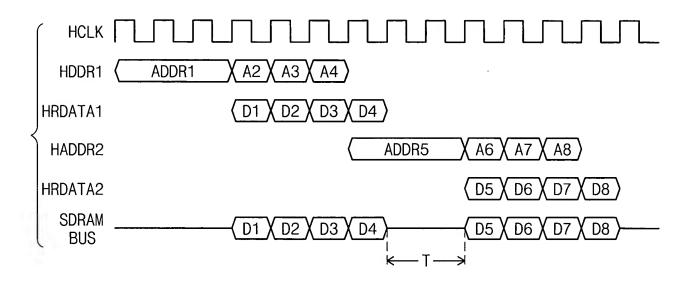
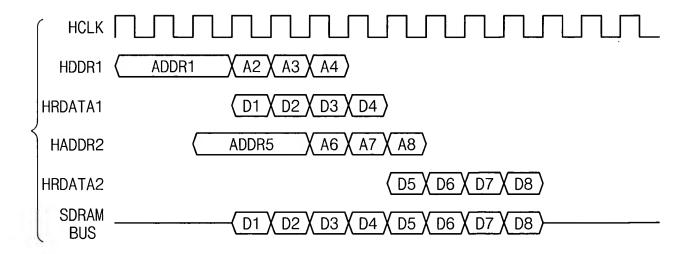


Fig. 2



Bank3 DATA Bank2 S controller SDRAM SDRAM BIREADYD HADDR, HWRITE, HBURST, HSIZE, HTRAN Bank1 BIWDATA BIRDATA Bank0 (9 HMASTER **ω** (Hgrant) 001 010 100 MX HMASTERf Arbitration logic (Select 1 master) HADDR2, HWRITE2, HBURST2, HSIZE2, HTRAN2 Š HADDR1, HWRITE1, HBURST1, HSIZE1, HTRAN HADDR3, HWRITE3, HBURST3, HSIZE3, HTRAN3 HBUSRE02 HBUSREQ3 HBUSREQ1 **HWDATA1** Master1 HGRANT1 **HRDATA1 HWDATA2** Master2 HGRANT2 HRDATA2 **HWDATA3** Master3 HGRANT3 HRDATA3

Fig. 3

Fig. 4

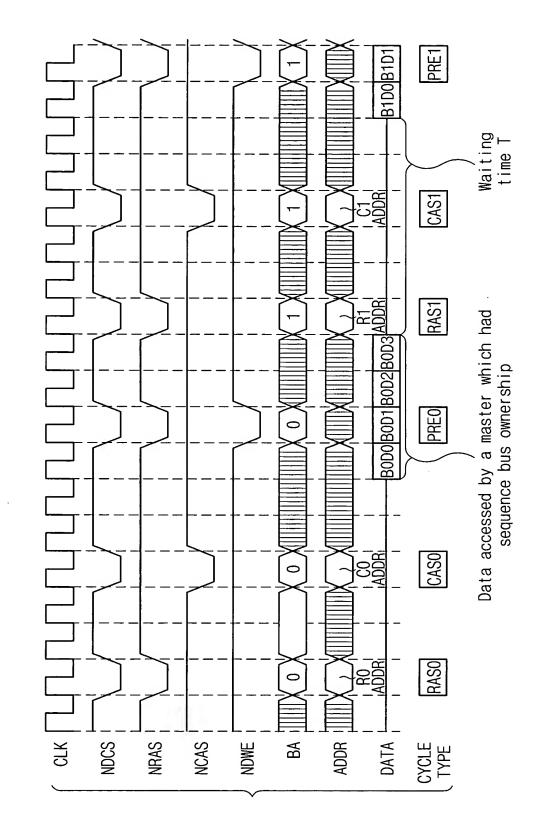


Fig. 5

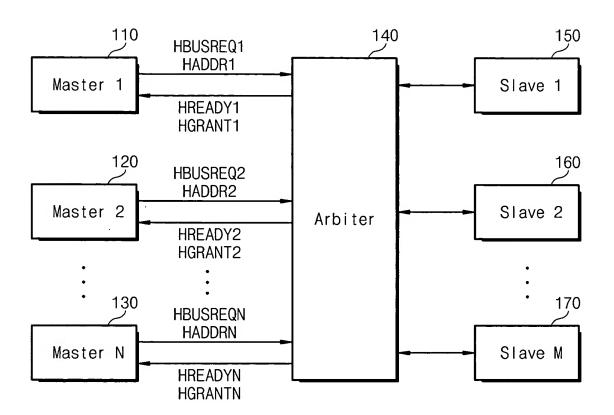
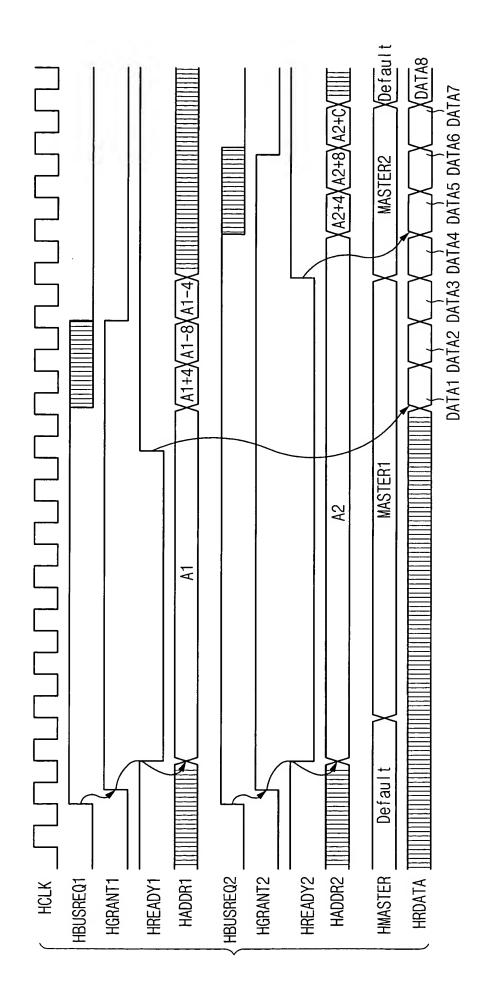


Fig. 6



DATA Slave 3 controller 543 က Slave 573 **BIRDATA3** DATA controller 542 \sim Slave 2 Slave 572 **BIRDATA2** DATA Slave 1 controller 541 Slave 571 **BIRDATA1** controller interface BIWDATA 550 554 Slave HMASTER ~560 -552 ¥ 580~ BIRDATA Master interface HBUSREQ2 HADDR2 HBUSRT2 HWRITE2 HBUSREQ3 HADDR3 HBUSRT3 HWR I TE3 HBUSREQ1 HADDR1 HBUSRT1 HWR I TE1 **HWDATA1** 510 Master1 HREADY1 HGRANT1 **HRDATA1 HWDATA2** Master2 HREADY2 HGRANT2 HRDATA2 HWDATA3 520 Master3 HREADY3 HGRANT3 530 HRDATA3

Fig. 7

244 Bank3 243 DATA Bank2 270 controller SDRAM SDRAM BIWDATA 242 Bank1 NDCS NRAS NCAS NCAS NDWE BA BA BIBA, BIBE, BIBA, BIBE, BIRDATA 241 Bank0 BIREADYD, BICONFIRMD 240~ SDRAM controller interface 254 HMASTER ~260 250 -252 $\widetilde{\mathbb{A}}$ Master interface HBUSREQ2 HADDR2 HBUSRT2 HWR I TE2 HBUSREQ3 HADDR3 HBUSRT3 HWR I TE3 HBUSREQ1 HADDR1 HBUSRT1 HWRITE1 **HWDATA1** 210 Master1 HREADY1 HGRANT1 **HWDATA2** HRDATA1 220 Master2 HREADY2 HGRANT2 HRDATA2 230 Master3 HREADY3 HGRANT3 HRDATA3

Fig. 8

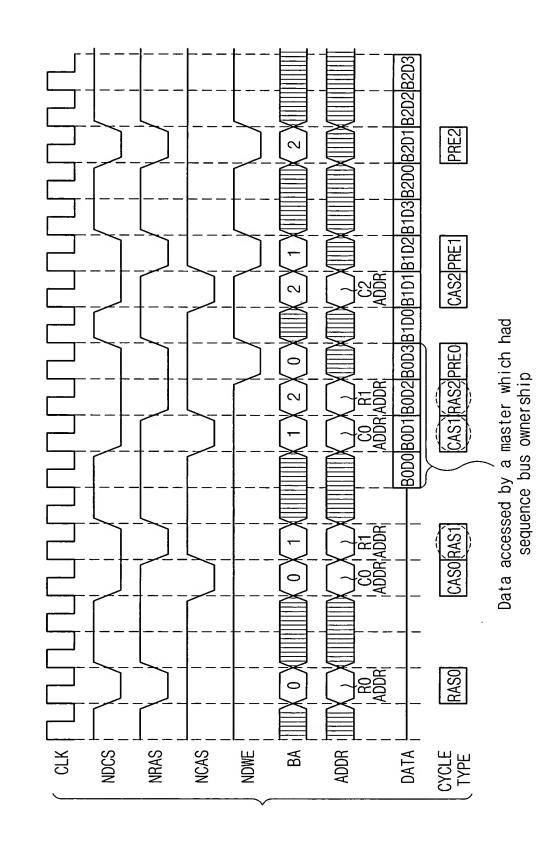


Fig. 10

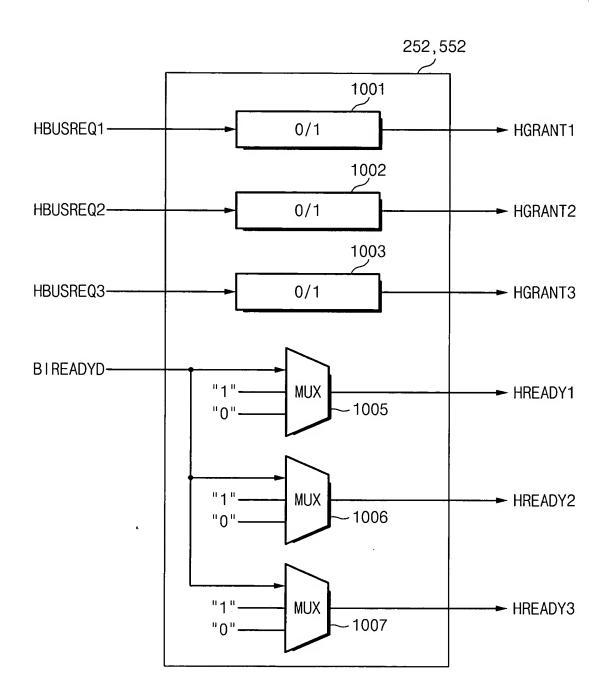


Fig. 11

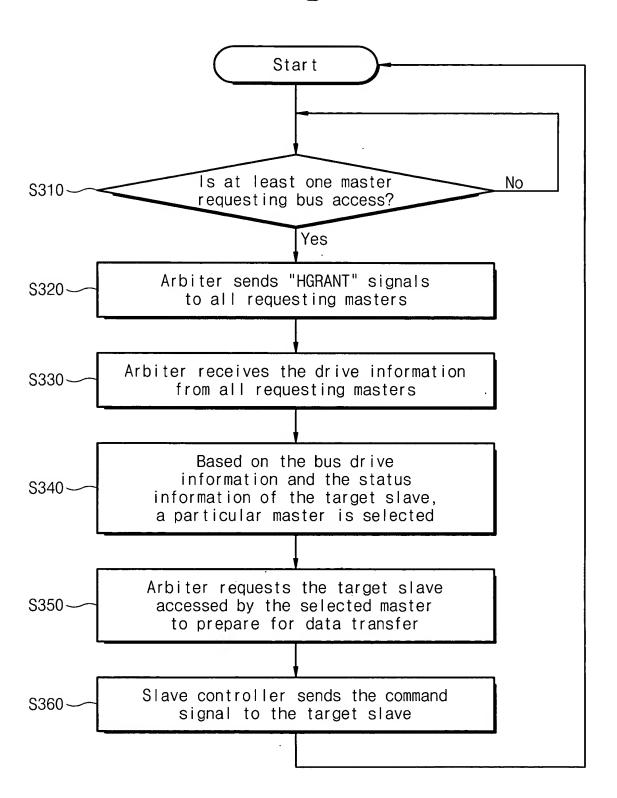


Fig. 12

